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# SLF65R600E7 / SLD65R600E7

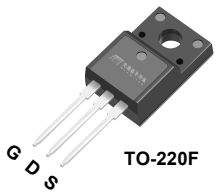
## 650V N-Channel Multi-EPI Super-JMOSFET

### General Description

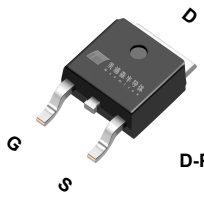
This Power MOSFET is produced using Msemitek's advanced Superjunction MOSFET technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies.

### Features

- 8A, 650V, $R_{DS(onTyp}$ =510mΩ@$V_{GS}$ = 10 V
- Low gate charge(typ. Qg =10.1nC)
- High ruggedness
- Ultra fast switching
- 100% avalanche tested
- Improved dv/dt capability




TO-220F

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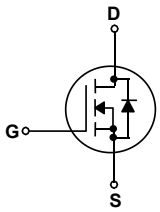



## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | SLF65R600E7 /SLD65R600E7 | | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 650 | | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25℃) | | 8* | | A |
| | - Continuous ($T_C$ = 100℃) | | 4.8* | | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 24* | | A |
| $V_{GSS}$ | Gate-Source Voltage | | ±30 | | V |
| EAS | Single Pulsed Avalanche Energy | (Note 2) | 22 | | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 1.9 | | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 0.61 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 20 | | V/ns |
| | MOSFET dv/dt | | 100 | | |
| $P_D$ | Power Dissipation ($T_C$ = 25℃) | | 24 | 69 | W |
| | - Derate above 25℃ | | 0.19 | 0.56 | W/℃ |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | | ℃ |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 260 | | ℃ |

* Drain current limited by maximum junction temperature.

## Thermal Characteristics

| Symbol | Parameter | SLF65R600E7 /SLD65R600E7 | | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 5.2 | 1.8 | ℃/W |
| $R_{\theta JS}$ | Thermal Resistance, Case-to-Sink Typ. | - | - | ℃/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 62.5 | 62.5 | ℃/W |

## Package Marking

| Part Number | Top Marking | Package | Packing Method | MOQ | QTY |
|---|---|---|---|---|---|
| SLF65R600E7 | SLF65R600E7 | T0-220F | Tube | 1000 | 5000 |
| SLD65R600E7 | SLD65R600E7 | T0-252 | Tape | 2500 | 25000 |

## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250uA | 650 | -- | -- | V |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250uA, $T_J$ = 150℃ | 650 | -- | -- | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | -- | -- | 1 | uA |
| | | $V_{DS}$ =480 V, $T_C$ = 125℃ | -- | 2.1 | -- | uA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250uA | 2.5 | -- | 4.5 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | -- | 510 | 600 | mΩ |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, f = 1MHz | -- | 383 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 20 | -- | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | -- | -- | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DS}$ = 400 V, $I_D$ =2.5 A, $R_G$ = 10 Ω,VGS = 10 V (Note 4, 5) | -- | 6 | -- | ns |
| $t_r$ | Turn-On Rise Time | | -- | 7 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 26 | -- | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 13 | -- | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 400 V, $I_D$ =2.5A, $V_{GS}$ = 10 V (Note 4, 5) | -- | 10.1 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 2.1 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 4.9 | -- | nC |
| $R_G$ | Gate Resistance | f = 1MHz | | 0.7 | | Ω |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 8 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 24 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.5A | -- | -- | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{DD}$ = 400 V, $I_S$ = 2.5A, $dI_F$ / dt = 100 A/us (Note 4) | -- | 173 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 1.1 | -- | uC |

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}$ = 1.9 A, $V_{DD}$ = 50V, $R_G$ = 25Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 2.5A, di/dt ≤ 200A/us, $V_{DD}$ ≤400, Starting $T_J$ = 25°C
4. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Characteristics

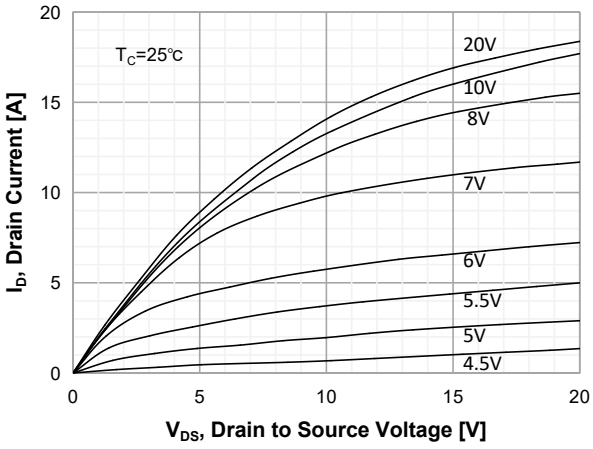



**Figure 1. On-Region Characteristics**

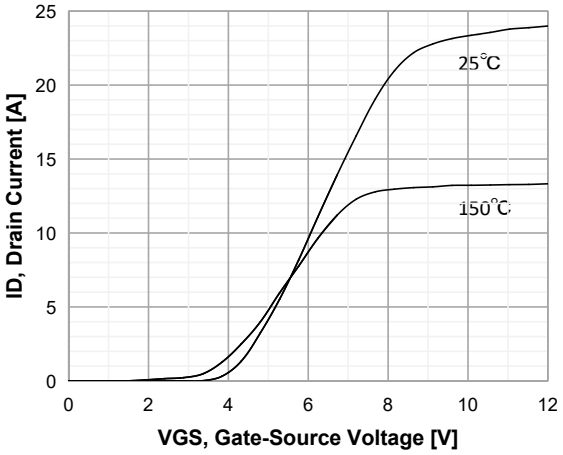



**Figure 2. Transfer Characteristics**

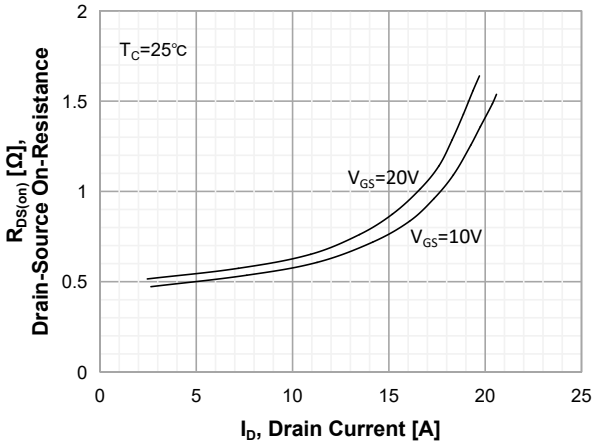



**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**

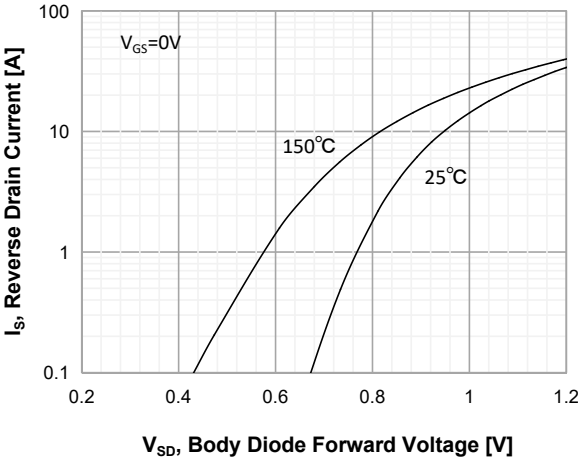



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

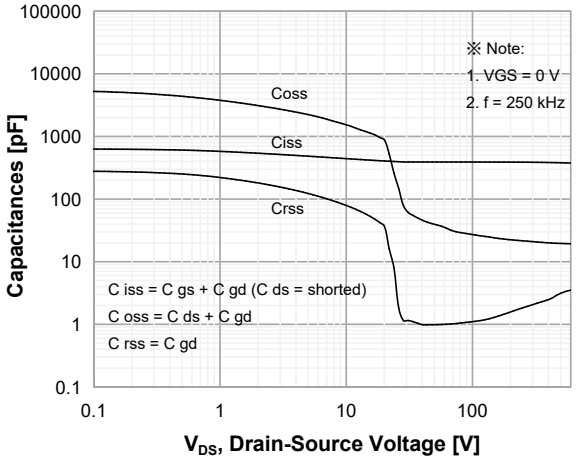



**Figure 5. Capacitance Characteristics**

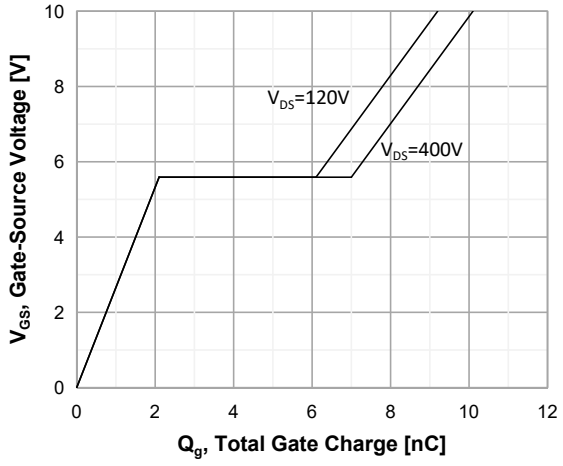



**Figure 6. Gate Charge Characteristics**

## Typical Characteristics (Continued)

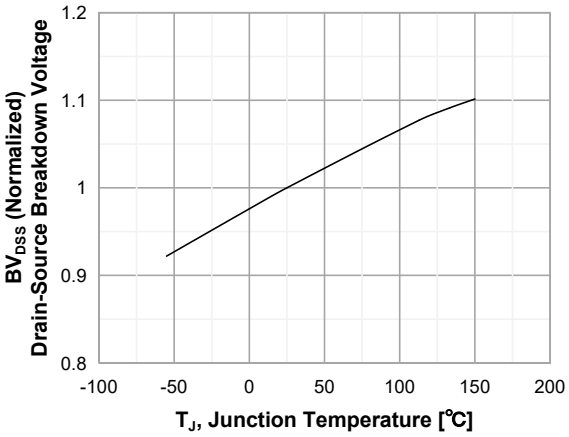



**Figure 7. Breakdown Voltage Variation vs Temperature**

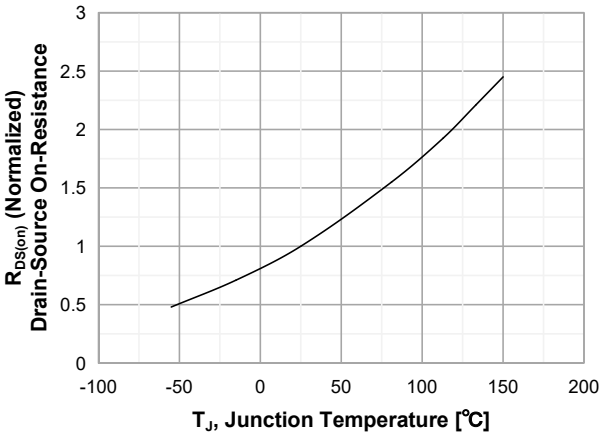



**Figure 8. On-Resistance Variation vs Temperature**

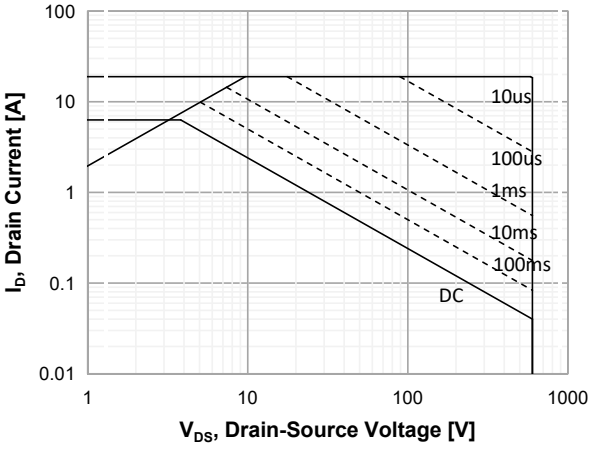



**Figure 9. Maximum Safe Operating Area**

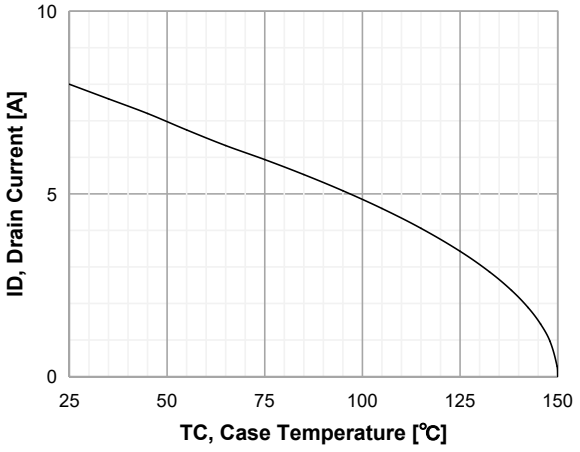



**Figure 10. Maximum Drain Current vs. Case Temperature**

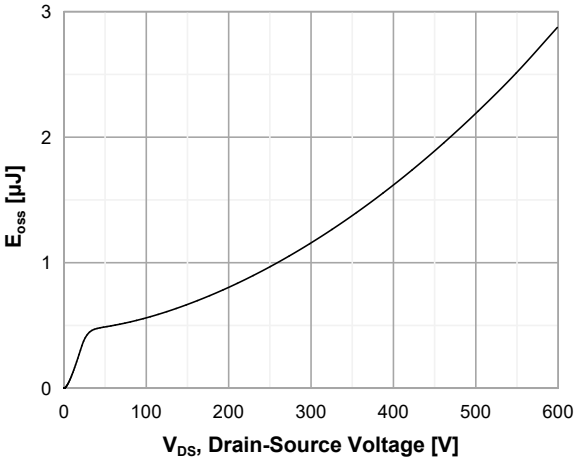



**Figure 11.$E_{oss}$ vs. Drain to Source Voltage**

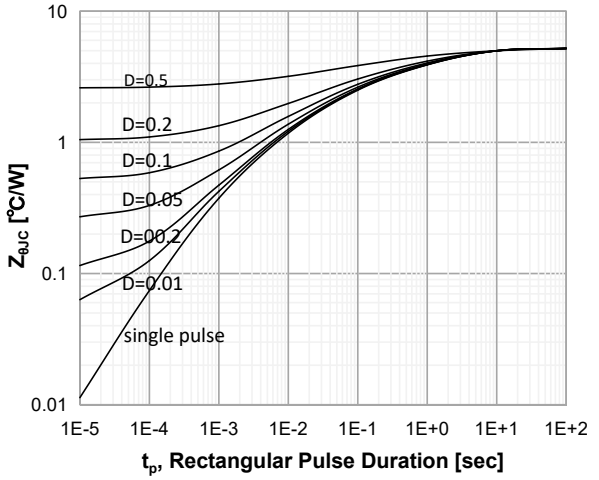
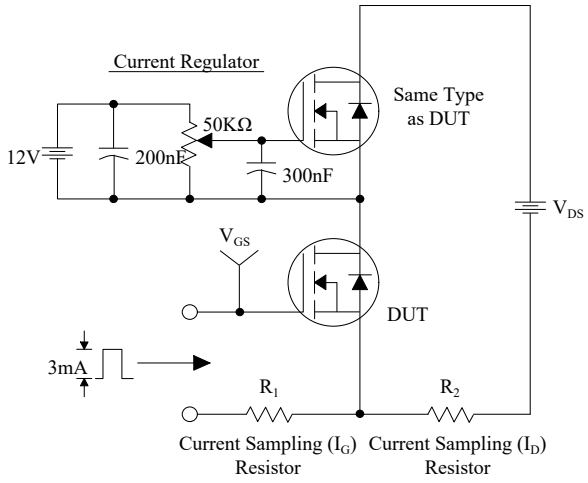
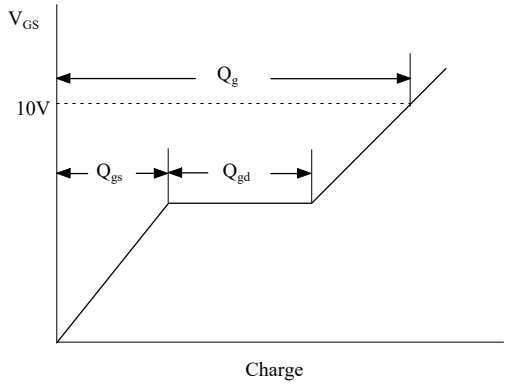


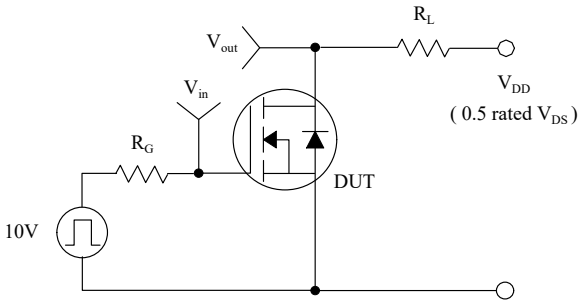

**Figure 12.Transient Thermal Response Curve**

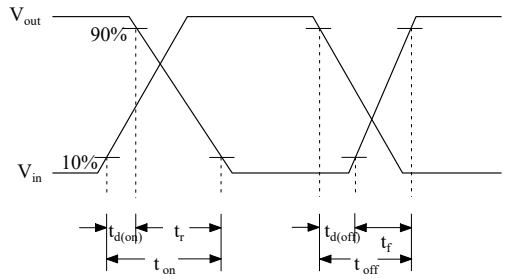
## Gate Charge Test Circuit & Waveform



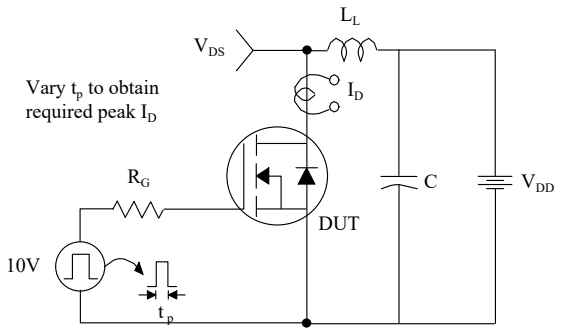




## Resistive Switching Test Circuit & Waveforms

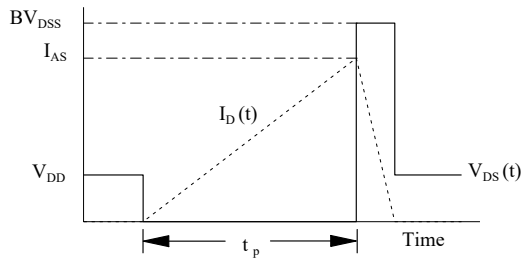


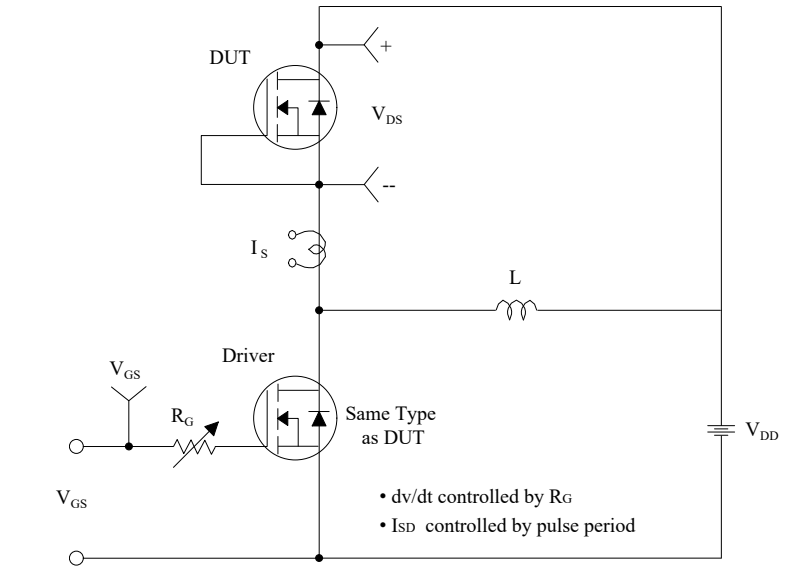

## Unclamped Inductive Switching Test Circuit & Waveforms

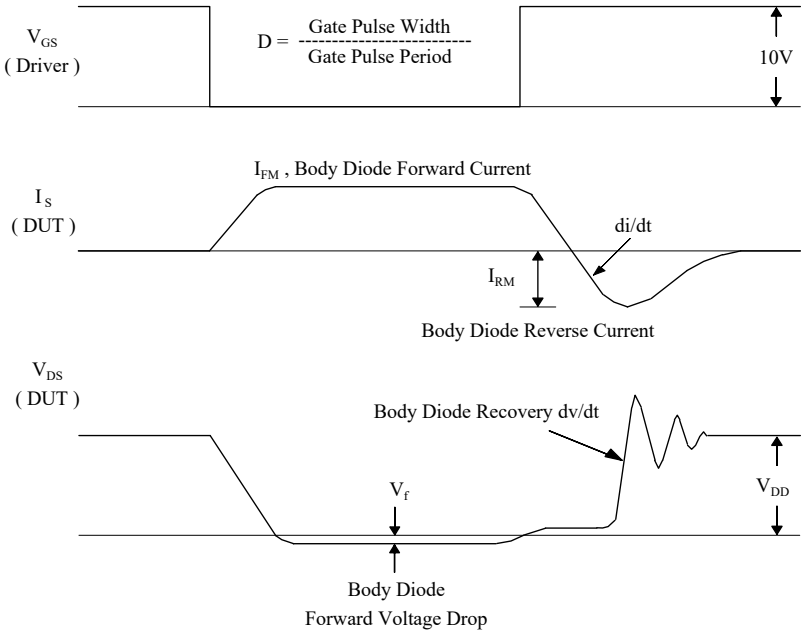



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

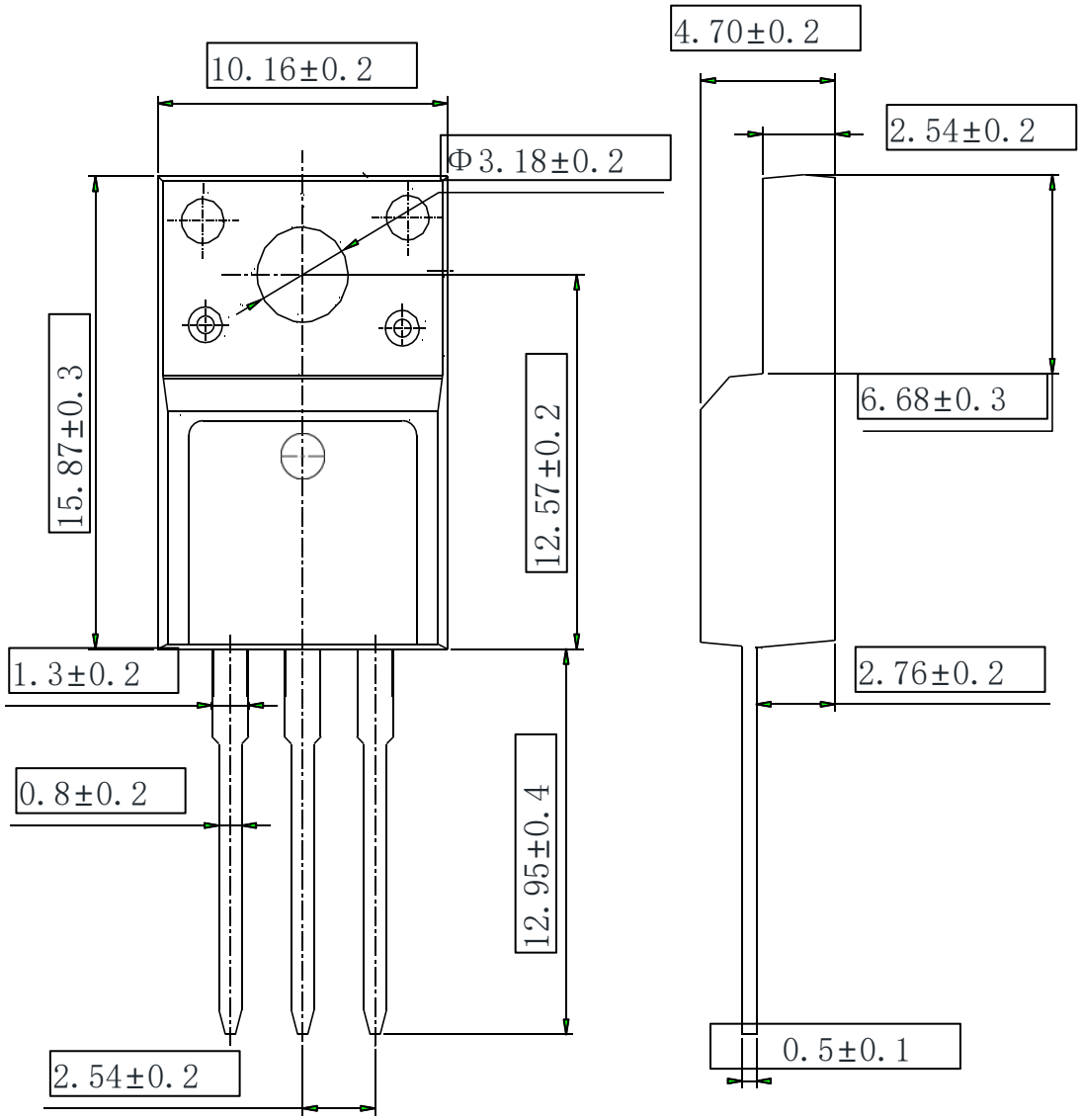


# Peak Diode Recovery dv/dt Test Circuit & Waveforms



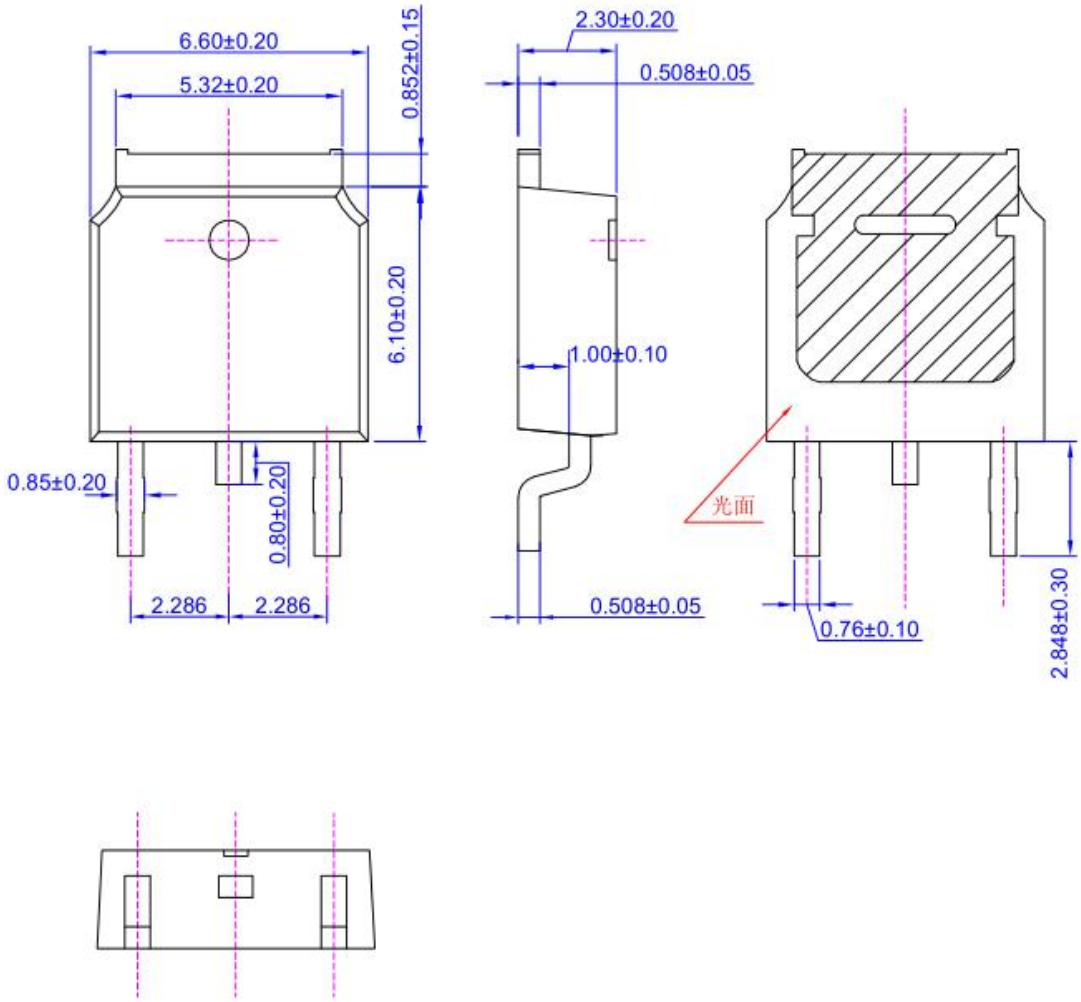



# TO-220F OUTLINE




NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

# TO-252 OUTLINE




NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

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