美浦森半导体
M s e m i t e k

RoHS
LEAD FREE

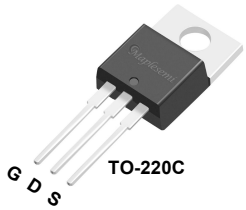
SLP20N65U / SLF20N65U
650V N-Channel MOSFET

General Description

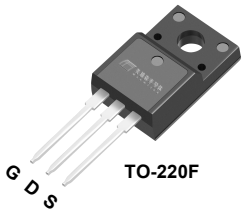
This Power MOSFET is produced using Msemitek's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

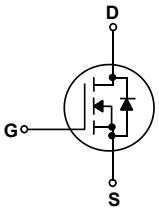
- 20A, 650V, $R_{DS(on)Type}$=0.4Ω@V_{GS} = 10 V
- Low gate charge (typical 50nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220C



TO-220F



Absolute Maximum Ratings T_C = 25℃ unless otherwise noted

Symbol	Parameter	SLP20N65U	SLF20N65U	Units
V_{DSS}	Drain-Source Voltage	650		V
I_D	Drain Current - Continuous (T_C = 25℃)	20		A
	Drain Current - Continuous (T_C = 100℃)	14		A
I_{DM}	Drain Current - Pulsed (Note 1)	70		A
V_{GSS}	Gate-Source Voltage	±30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	185		mJ
P_D	Power Dissipation (T_C = 25℃)	208	45	W
	- Derate above 25℃	1.67	0.36	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		℃

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLP20N65U	SLF20N65U	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.60	2.78	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	℃/W

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLP20N65U	SLP20N65U	T0-220C	Tube	1000	5000
SLF20N65U	SLF20N65U	TO-220F	Tube	1000	5000

Electrical Characteristics

T_C = 25℃unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 10A	--	0.4	0.58	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	2570	--	pF
C_{oss}	Output Capacitance		--	220	--	pF
C_{rss}	Reverse Transfer Capacitance		--	7.7	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400V,V_{GS} = 10V, I_D =20A, R_G = 20 Ω (Note 3)	--	96	--	ns
t_r	Turn-On Rise Time		--	46	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	91	--	ns
t_f	Turn-Off Fall Time		--	32	--	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 20A, V_{GS} = 10 V (Note 3)	--	50	--	nC
Q_{gs}	Gate-Source Charge		--	13.4	--	nC
Q_{gd}	Gate-Drain Charge		--	17.8	--	nC
R_G	Gate Resistance	f = 1MHz		2		Ω
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	20	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	80	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S =20A	--	--	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S =20A, dI_F / dt = 130 A/us	--	477	--	ns
Q_{rr}	Reverse Recovery Charge		--	8	--	uC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V_{DD} =50V, V_G =10V, L=0.5mH,
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

N- Channel Typical Characteristics

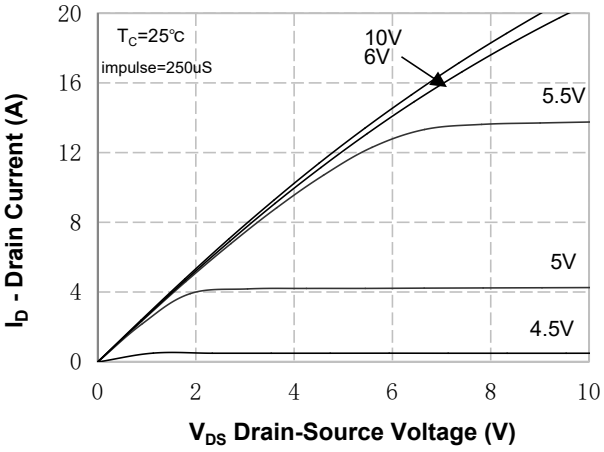


Figure 1. On-Region Characteristics

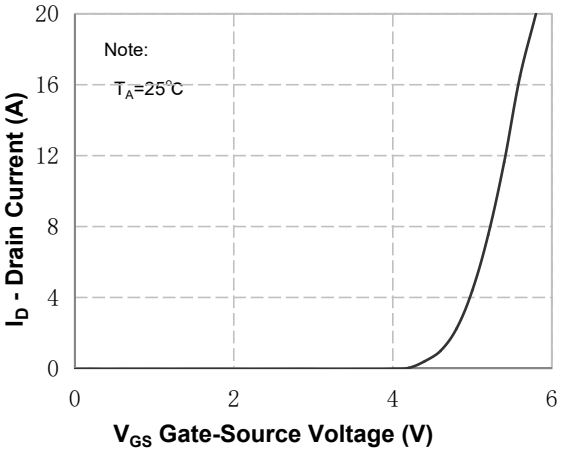


Figure 2. Transfer Characteristics

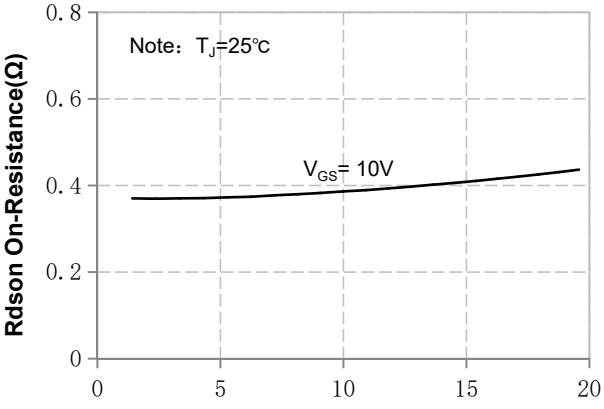


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

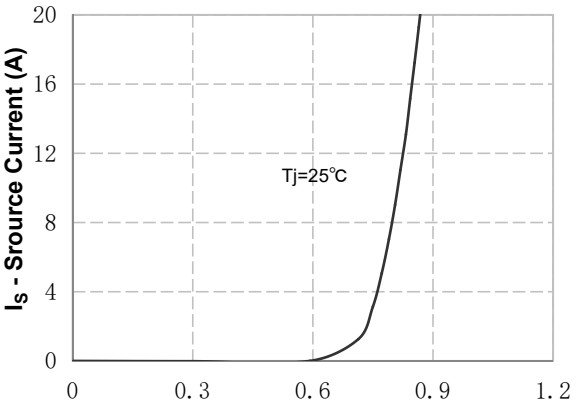


Figure 4. Source Current vs Source-Drain Voltage

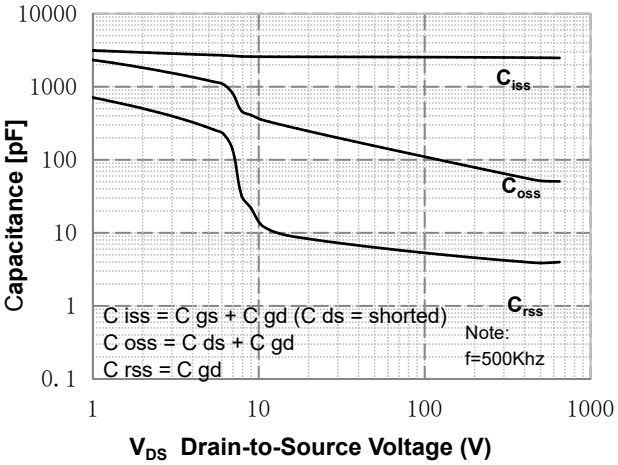


Figure 5.1 Capacitance Characteristics

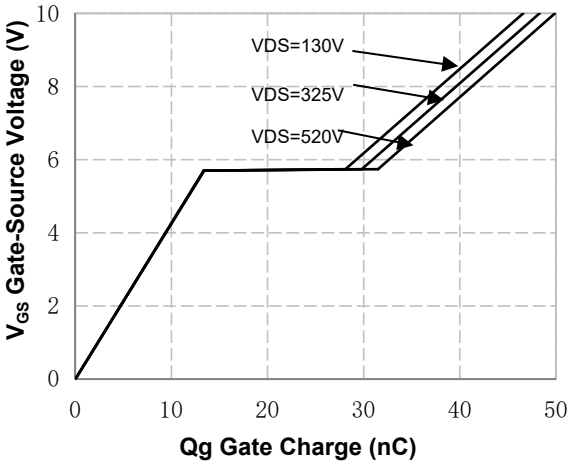


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

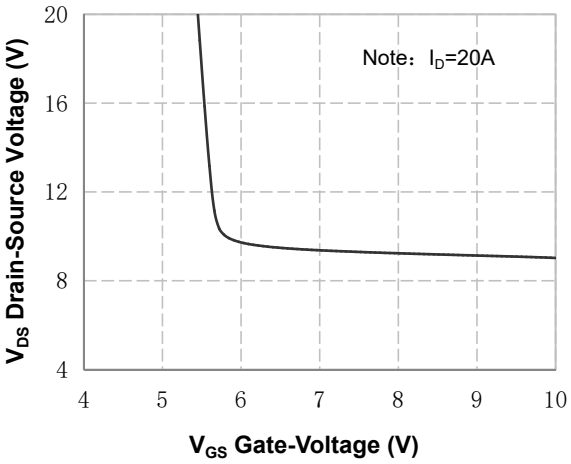


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

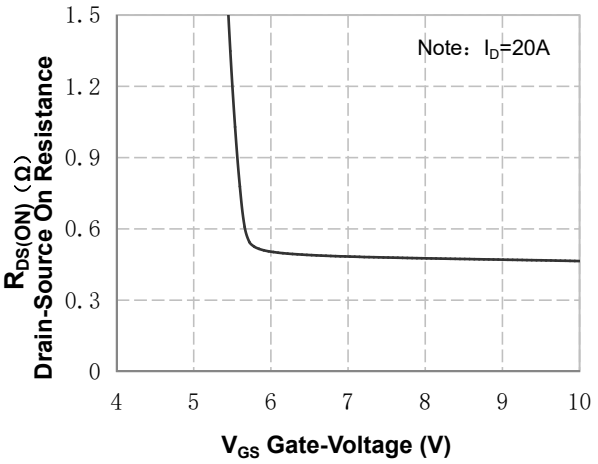


Figure 8. On-Resistance vs Gate Voltage

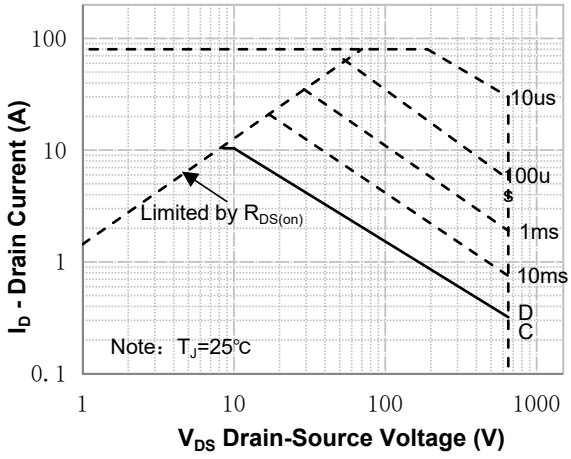


Figure 9. Maximum Safe Operating Area

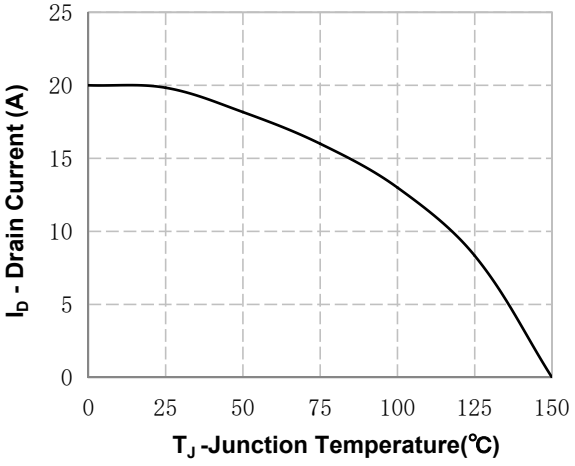


Figure 10. Maximum Drain Current vs Temperature

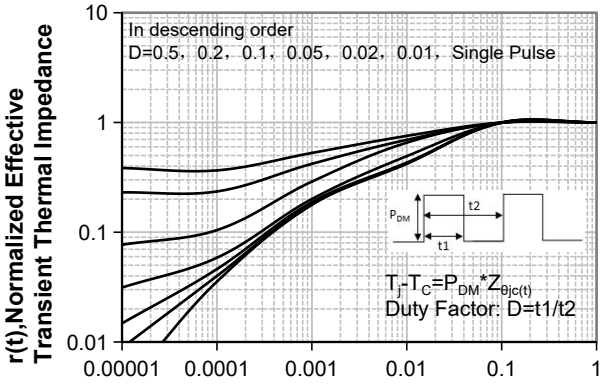
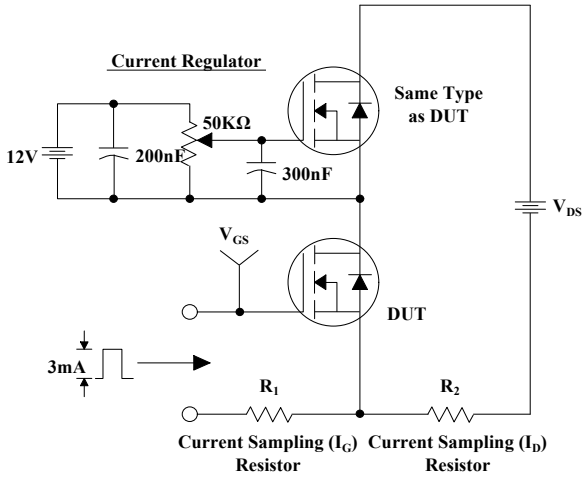
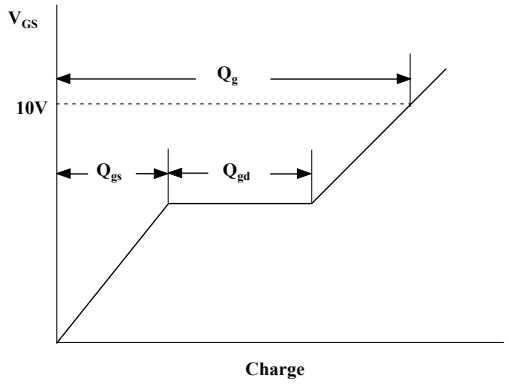


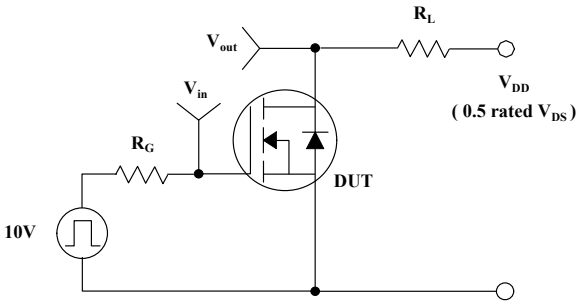
Figure 11. Transient Thermal Response Curve

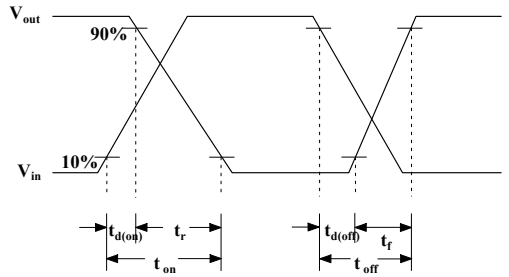
Gate Charge Test Circuit & Waveform



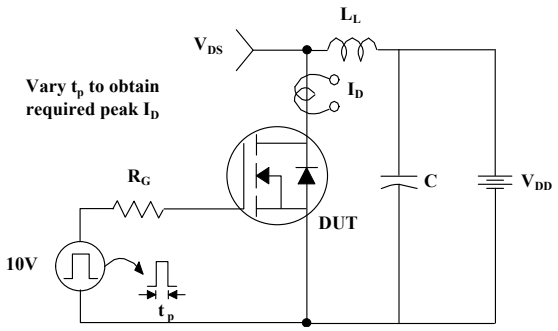


Resistive Switching Test Circuit & Waveforms

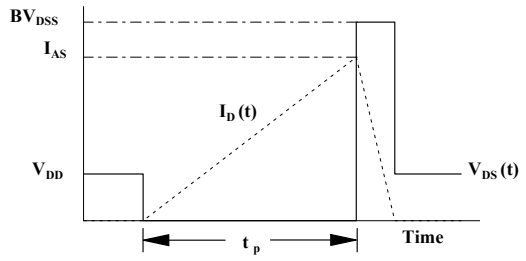




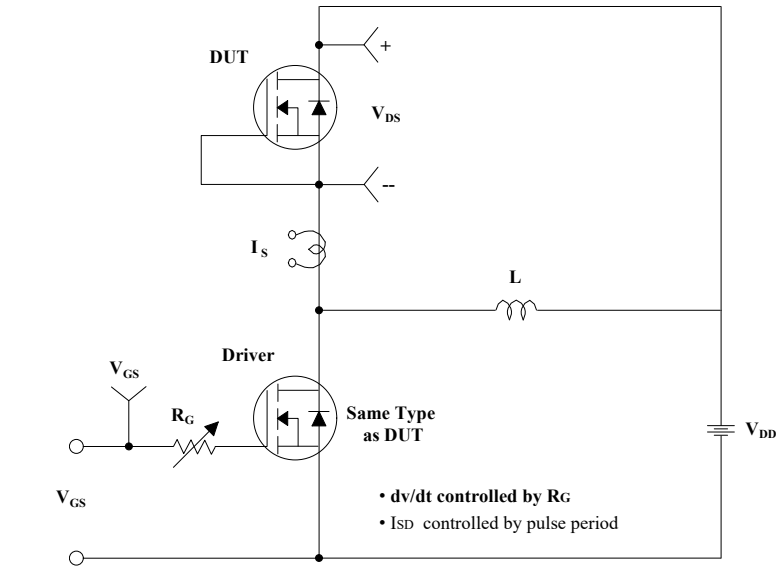
Unclamped Inductive Switching Test Circuit & Waveforms

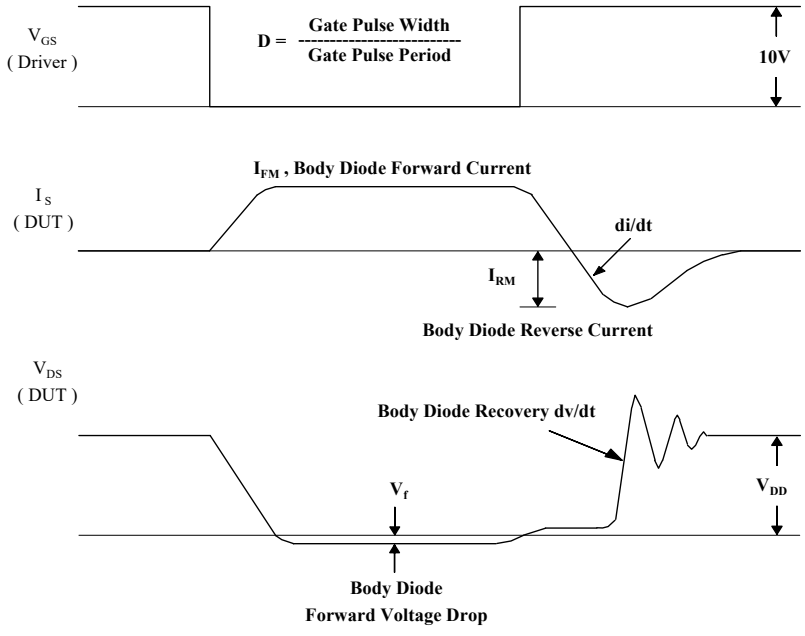


$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

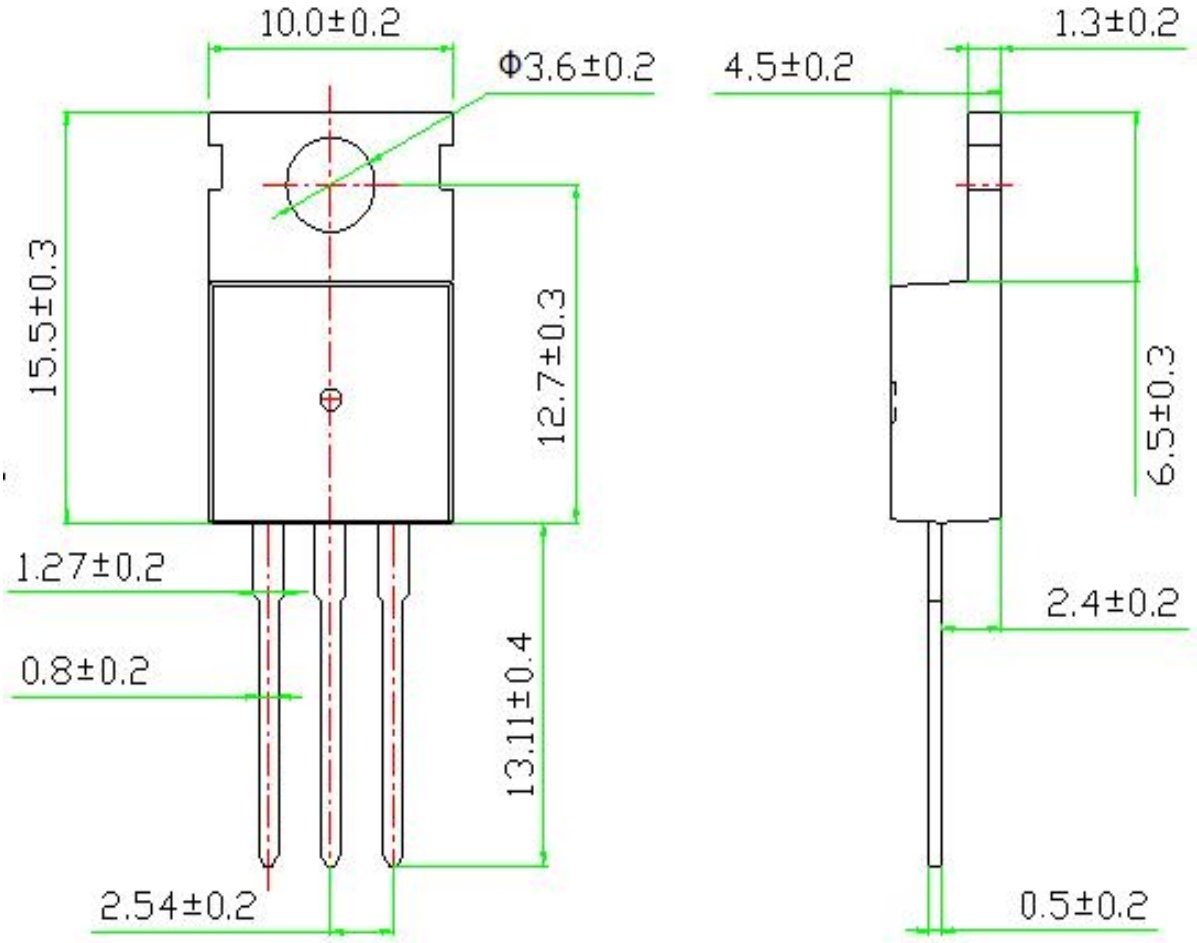


Peak Diode Recovery dv/dt Test Circuit & Waveforms



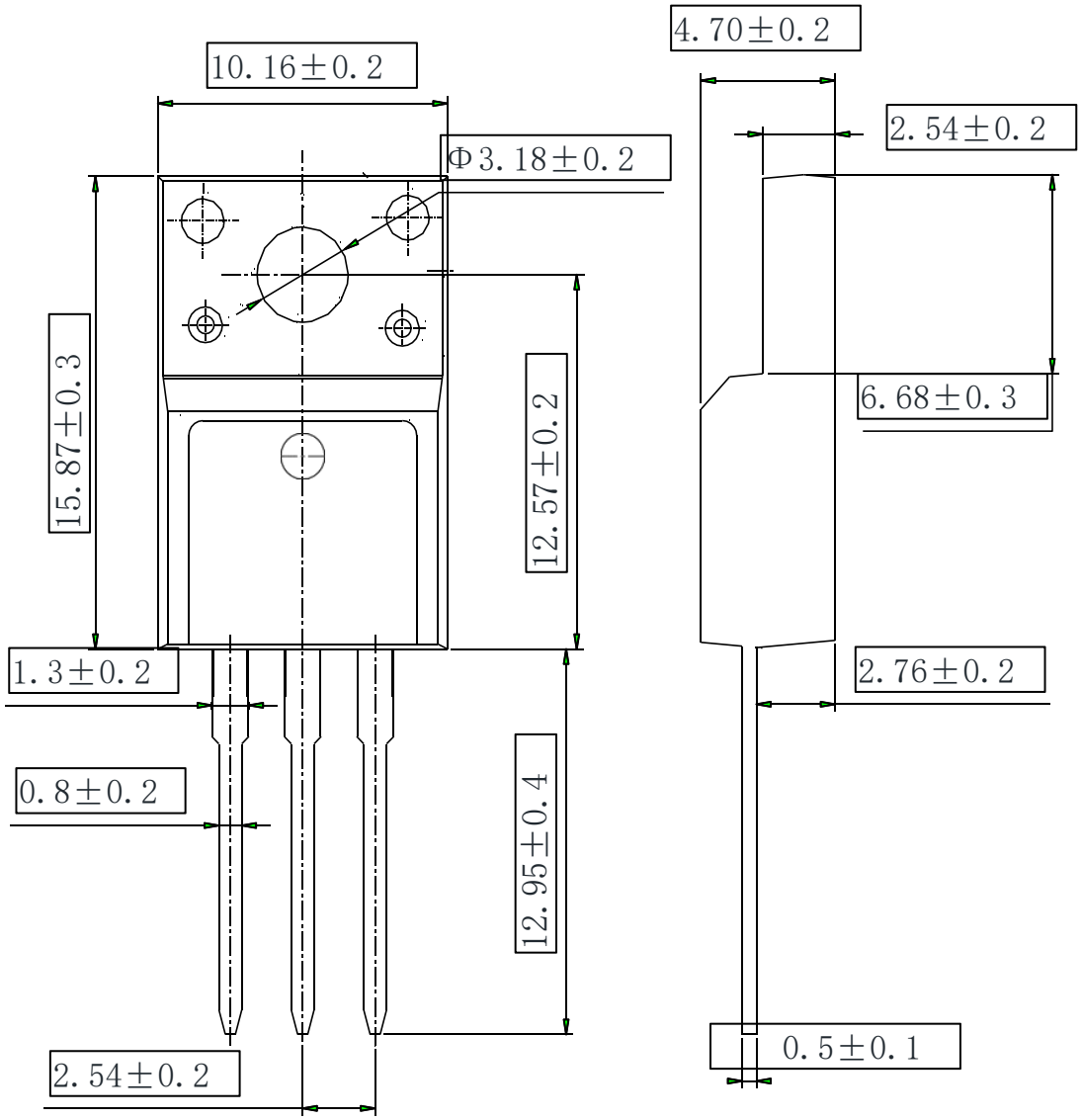


TO-220C OUTLINE



NAME	TO-220C OUTLINE	UNIT	mm	DESIGNED	Shawn Chen	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

TO-220F OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

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